Standard PCI LEON Virtex-5
Development Board
GR-PCI-XC5V

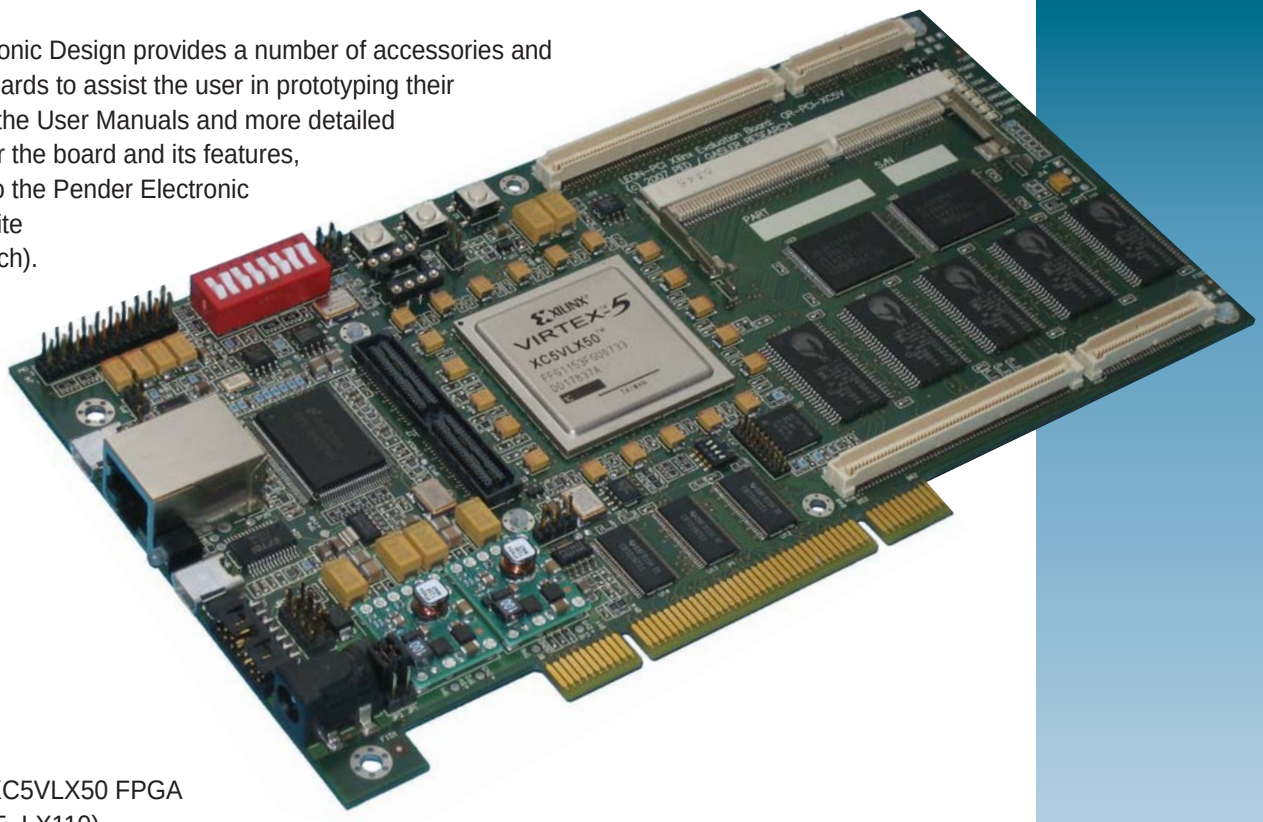
AEROFLEX GAISLER

Description

In cooperation between Aeroflex Gaisler and Pender Electronic Design the GR-PCI-XC5V FPGA development board has been conceived especially to support development and fast prototyping of systems based on the LEON processors. The board incorporates a large capacity Xilinx Virtex-5™ field programmable gate array and is capable of operating stand-alone, as a PCI plug-in card, or can be configured as a PCI host in passive PCI backplane applications.

Whilst the board is perfectly suitable as a general purpose development platform for any Xilinx project, the incorporation of on-board volatile (SRAM and SDRAM) and non-volatile memories (FLASH), together with Serial, Ethernet and USB interfaces makes the board ideal for implementing LEON3 and LEON4 designs. Additionally, the design of this board can support the implementation of LEON-FT fault-tolerant systems.

Pender Electronic Design provides a number of accessories and mezzanine boards to assist the user in prototyping their systems. For the User Manuals and more detailed information for the board and its features, please refer to the Pender Electronic Design web-site (www.pender.ch).



Features

- Virtex-5™, XC5VLX50 FPGA (option: LX85, LX110)
- PCI plug-in format (33 MHz, 32-bit)
- On-board memory:
  - SRAM
  - SDRAM SODIMM module
  - FLASH PROM
- Debug Support Unit interface (USB/RS232)
- Mezzanine expansion options: Mil-Std 1553B, ADC/DAC, CAN
- User I/O Connectors
- Ethernet PHY GBIT transceiver (DP83865)
- USB 2.0 ULPI Host / Peripheral Interface (ISP1504)
- On-board oscillators
- FPGA configuration and programming via JTAG
- Specially designed and configurable for LEON core implementations
- Capable of supporting LEON-FT core implementations
- PIO expansion options: RS232 / RS422 / LVDS / CAN / TM & TC
- Dedicated high speed connectors

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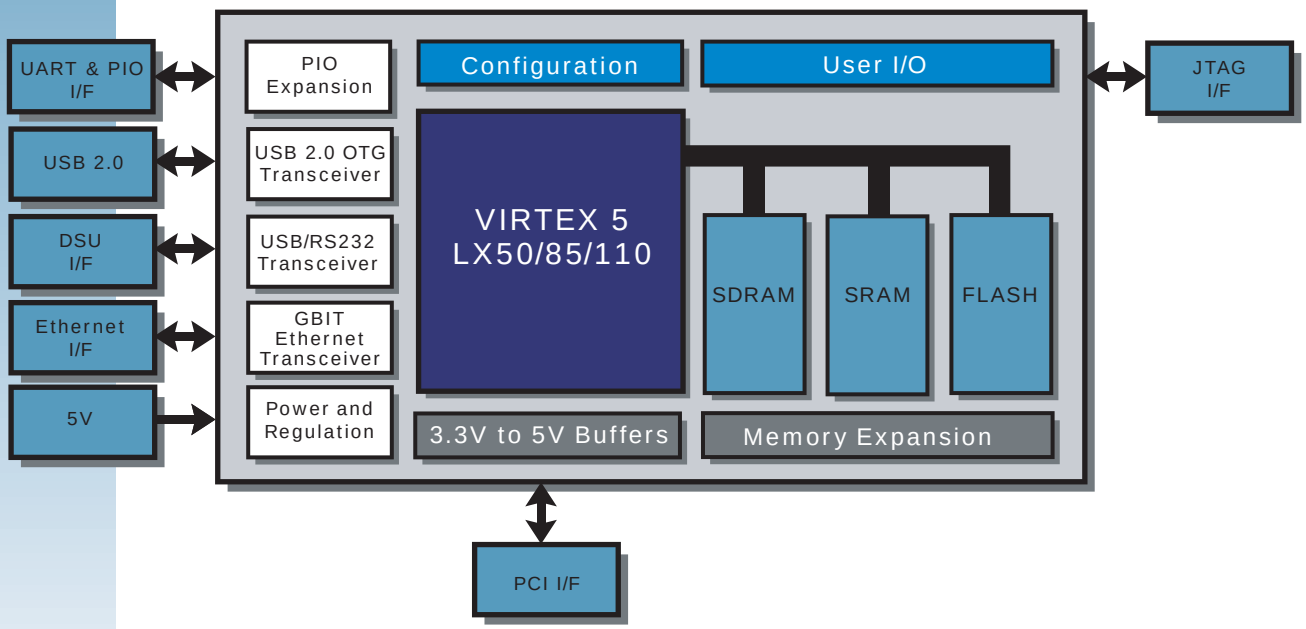
LEON Applications and Support

The LEON processor is a synthesisable VHDL model of a 32-bit processor compliant with the SPARC V8 architecture. The LEON processor, both as an FPGA and as an ASIC has been incorporated in numerous Aerospace, Industrial and Consumer electronic designs. The LEON design is unique in its source-code availability, offering the user extensive configuration options and full flexibility in the use and extension of the core's functions to suit the user's specific application and interfaces.

For more information on the LEON core, the VHDL model, synthesis, configuration, hardware and software development tools, IP core developments and Real-Time Operating Systems, please refer to the Aeroflex Gaisler web-site (www.aeroflex.com/gaisler).

Specifications

- XC5VLX50 Xilinx Virtex-5 FPGA (standard option)
- Typical core speeds 50 to 100 MHz (depending on speed grade and core configurations)
- On-board FPGA configuration PROM (XCF32P)
- Standard memory options:
  - SDRAM, SODIMM (64 bit wide up to 512 MByte)
  - SRAM, on-board 80 Mbit (2 Mword x 40 bit)
  - FLASH PROM, on-board 128 Mbit (4 Mword x 32 bit)
- 33 MHz, 32-bit PCI
- 10/100/1000 Mbit Ethernet PHY and RJ45 connector
- USB-MiniAB connector for USB 2.0 OTG transceiver
- USB-MiniAB connector for DSU/UART I/F
- Memory and user I/O expansion connectors with 60 and 120 pin connectors (AMP 177-984-2/5) compatible with our CPCI mezzanine boards



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