

USB 2.0 Host Controller

High-, Full- and Low-Speed USB Host IP Core

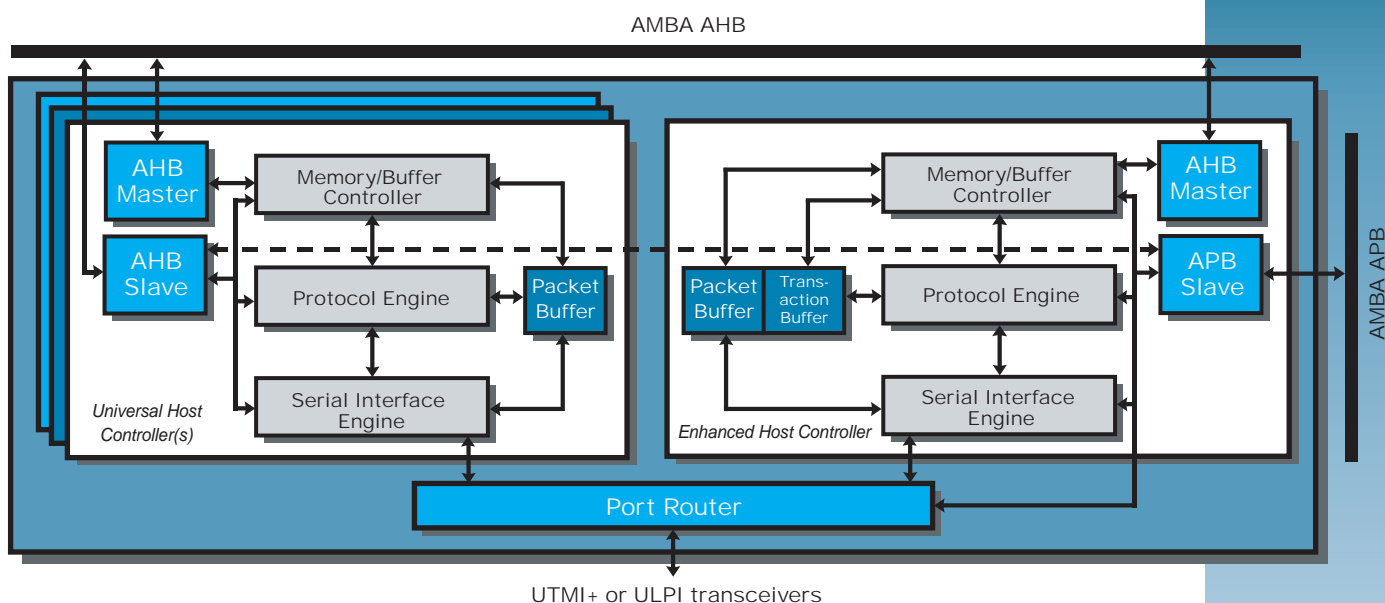


Description

The USB 2.0 Host Controller core (GRUSBHC) provides a link between the AMBA on-chip bus and the Universal Serial Bus (USB). The host controller supports High-, Full- and Low-Speed USB traffic. USB 2.0 High-Speed functionality is supplied by an enhanced host controller implementing the Enhanced Host Controller Interface (EHCI). Full- and Low-Speed functionality (USB 2.0 and USB 1.1) is supplied by one or more companion controllers implementing the Universal Host Controller Interface (UHCI). The Port Router supplies the dynamic connection between the host controllers and the USB transceivers.

The core can handle up to 15 downstream ports, where each port can handle all three USB speeds. Port routing within the core is highly configurable. The designer has choices ranging from handling Full/Low-Speed traffic with one companion controller per port, to having one companion controller handle all ports. The modularity of the core enables the designer to configure High- or Full/Low-Speed only products. Both controller types have support for big and little endian systems, with the option to adjust the register interfaces' byte order to fit the target platform.

The core supports UTMI+ 16-bit transceivers at 30 MHz and 8-bit transceivers at 60 MHz, and ULPI 8-bit transceivers at 60 MHz.



Features

- Compatible with USB Specification Rev. 2.0 and Rev. 1.1
- Supports all USB transfer types
- Supports High- (480 Mbit/s), Full- (12 Mbit/s) and Low-Speed (1.5 Mbit/s) traffic
- Enhanced Host Controller compatible with EHCI rev. 1.0
 - Supports Asynchronous Park Mode
 - Implements a NAK counter to limit unnecessary memory accesses
 - Descriptor and data prefetch prevents buffer overrun and underrun errors
 - AMBA AHB 32-bit master interface, APB 32-bit slave interface
- Universal Host Controller compatible with UHCI rev. 1.1
 - Extended to report over current conditions
 - AMBA AHB master/slave interface
 - Flexible configuration of port routing and number of companion controllers
- Supports up to 15 downstream ports with up to 127 devices each
- Easily adaptable to both big and little endian systems
- Supports UTMI+ and ULPI transceivers
- AMBA DMA interface with configurable burst length
- AMBA Specification Rev. 2.0 compatible

Benefits

- Fully compatible USB 2.0 core
- USB Rev. 1.1 controller supports multiple ports
- Fully integrated in the GRLIB IP library, including AMBA plug&play interface
- Stand-alone usage supported
- Evaluation boards available
- Low-cost commercial license

Deliverables

- VHDL RTL source code or FPGA/ASIC netlist
- Synthesis scripts
- Stand-alone testbench
- User's manual
- Drivers for Linux 2.6

Size and performance

Core configuration	Number of ports	Xilinx Virtex 4* (Cells / RAM / MHz)	ASIC gates
Universal host controller (USB Full- and Low-Speed traffic only)	1	3000 / 1 / 80 MHz	25000
Enhanced host controller (USB High-Speed traffic only)	1	9000 / 3 / 80 MHz	70000
Enhanced host controller with one universal companion controller** (supports all USB traffic speeds)	1	12000 / 3 / 80 MHz	95000
	2	13000 / 4 / 80 MHz	105000
	4	15000 / 4 / 80 MHz	125000
	8	20000 / 4 / 80 MHz	155000
	12	24000 / 4 / 80 MHz	195000
	15	27000 / 4 / 80 MHz	215000

* (LUTs / RAM blocks / AHB system clock MHz)

** The single companion controller handles all ports.

The core can also be configured to include multiple companion controllers.

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