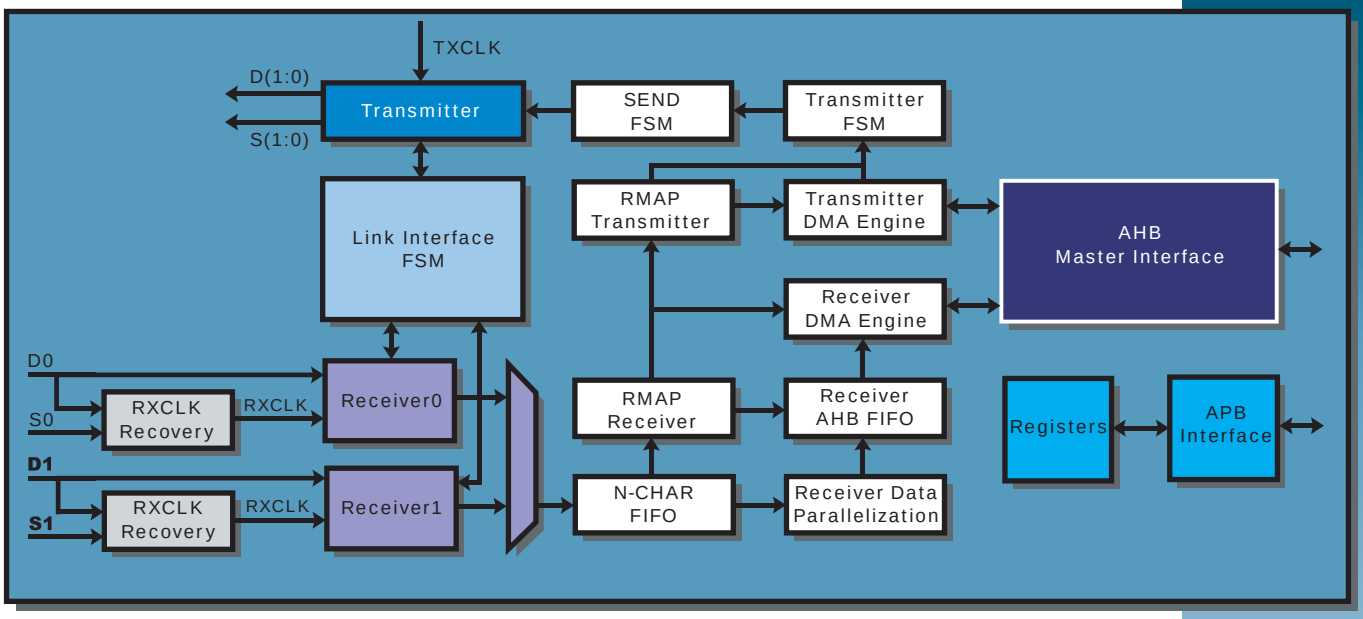
GRSPW
SpaceWire Link-interface

AEROFLEX GAISLER

Description

The GRSPW core implements a SpaceWire Codec with RMAP target and AMBA host interface. The core implements the SpaceWire standard (ECSS-E-ST-50-12C) with the protocol identification extension (ECSS-E-ST-50-51C) and RMAP protocol (ECSS-E-ST-50-52C). Receive and transmit data is autonomously transferred between the SpaceWire Codec and the AMBA AHB bus using DMA transfers. Through the use of receive and transmit descriptors, multiple SpaceWire packets can be received and transmitted without CPU involvement. The GRSPW control registers are accessed through an AMBA APB interface. For critical space applications, a fault-tolerant (FT) version of GRSPW is available with full SEU protection of all RAM blocks.



The GRSPW is inherently portable and can be implemented on most FPGA and ASIC technologies. The table below shows the approximate Cell/LUT count and frequency for seven different GRSPW configurations on Actel RTAX and RT ProAsic3, Xilinx Spartan3 and Virtex5 and ASIC technologies.

Size and Performance

RT ProAsic3 (Total core cells / Registers / AHB MHz / SpaceWire MHz / RAM)
RTAX (Total cells / R-cells / AHB MHz / SpaceWire MHz / RAM)
Spartan3 (LUTs / Registers / AHB MHz / SpaceWire MHz / RAM)
Virtex5 (LUTs / Registers / AHB MHz / SpaceWire MHz / RAM)

Core configuration	RTAX	RT ProAsic3	Spartan3	Virtex5	ASIC
GRSPW	3400 / 1100 / 70 / 180 / 3	4800 / 1100 / 65 / 120 / 5	2000 / 1000 / 75 / 180 / 2	1400 / 1000 / 170 / 400 / 3	10,000 gates
GRSPW + RMAP (1)	5100 / 1400 / 60 / 180 / 4	7500 / 1300 / 50 / 120 / 6	3300 / 1300 / 75 / 180 / 3	2300 / 1300 / 150 / 400 / 3	18,000 gates
GRSPW + 2P (2)	3700 / 1200 / 70 / 180 / 3	5200 / 1200 / 60 / 120 / 5	2200 / 1200 / 75 / 180 / 2	1500 / 1100 / 170 / 400 / 3	11,000 gates
GRSPW + RMAP + 2P	5400 / 1500 / 60 / 170 / 4	8000 / 1500 / 60 / 120 / 6	3500 / 1400 / 70 / 180 / 3	2500 / 1400 / 150 / 400 / 5	18,000 gates
GRSPW-FT (3)	3500 / 1100 / 65 / 170 / 5	5100 / 1100 / 50 / 120 / 10	2200 / 1100 / 75 / 180 / 5	1500 / 1000 / 150 / 400 / 5	11,000 gates
GRSPW-FT + RMAP	5200 / 1400 / 60 / 170 / 6	7800 / 1300 / 50 / 120 / 12	3500 / 1300 / 70 / 180 / 6	2400 / 1300 / 140 / 400 / 6	18,000 gates
GRSPW-FT + RMAP + 2P	5600 / 1500 / 60 / 170 / 6	8200 / 1500 / 50 / 120 / 12	3700 / 1500 / 70 / 180 / 6	2600 / 1400 / 140 / 400 / 6	18,000 gates

(1) Includes the RMAP target, (2) Dual SpaceWire ports. One is available in the standard configuration,
(3) Fault tolerant version

Features:	• Full implementation of SpaceWire standard ECSS-E-ST-50-12C • Protocol ID extension ECSS-E-ST-50-51C • Optional RMAP target ECSS-E-ST-50-52C • AMBA AHB back-end with DMA • Descriptor-based autonomous multi-packet transfer • Low area and high frequency • SEU protection fault-tolerance • Portable design • 3,000 Cells on RTAX2000S FPGA, 10,000 ASIC gates • 100 Mbit/s on RTAX2000S FPGA, 400 Mbit/s on ASIC • Netlist delivery • Configurable with one or two SpaceWire ports
Benefits:	• Tested and verified against several other SpaceWire cores • Low area and high frequency • Easily portable between FPGA and ASIC • Low-cost project license • SEU protection of all RAM blocks
Deliverables:	• FPGA/ASIC netlist • Stand-alone testbench • Optional plug&play interface for GRLIB IP Library • User's Manual • Driver for RTEMS and VxWorks

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