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LEON3-FT-RTAX SEU test results

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1 Introduction

1.1 Scope

This document describes the results of the heavy-ion testing of the LEON3FT processor implemented on a Actel RTAX-2000S device. The tests were performed during 28 November - 5 December 2005, using a Californium-252 SEU test system.

1.2 Summary

The LEON3-FT processor has been implemented in an RTAX-2000S FPGA, and subjected to heavy-ion error injection using Californium (Cf-252). The tests were carried out for 168 hours, with a flux of ~ 22 particles/s/cm^2 at the device surface. No computational errors, resets or other anomalies occurred and nominal operation was obtained during the full 168 hours of testing. The on-chip monitoring logic reported a total of 2,429 detected and corrected errors in the on-chip RAM blocks, resulting in an effective SEU rate of ~ 0.25 errors/minute. These results verified that the fault-tolerance features in LEON3-FT-RTAX are able to detected and correct more than 99.95% of all effective SEU errors under standard operating conditions (20 MHz, 50˚C).

By correlating the obtained Cf-252 SEU test data with simulated SEU injection, it was possible to determine the SEU cross-section for an RTAX2000S block RAM bit to 2.3E-9 cm^2/bit. This value corresponds well with earlier cross-section measurement performed by Actel at the BNL and TAMU cyclotron facilities, confirming the validity of the Cf-252 test methodology and obtained results.

The overall results shows that the fault-tolerance features included in the LEON3-FT-RTAX processor are well adapted to mitigate the SEU effects encountered in the space environment and provide a fault-free processing platform for both payload and platform applications.

2 LEON3-FT SPARC V8 Processor

2.1 Overview

The LEON3-FT SPARC V8 processor is a new implementation of the SPARC V8 architecture, consisting of a 7-stage pipeline, separate multi-set caches, and a fast, purely parity-based, SEU error-correction scheme. The deep pipeline and fast error-correction scheme allows frequencies up to 400 MHz on a standard 0.13 µm process, and up to 130 MHz on a Virtex2pro FPGA. On Actel RTAX devices, 25 - 30 MHz can be reached depending on device type and processor configuration. The processor core, consisting of the pipeline, cache controllers and AHB interface, consumes approximately 20% of the resources of an RTAX2000S device. A complete SOC design comprising of a LEON3 core, PROM/SRAM controller, SDRAM controller, timers, UARTs and interrupt controller, consumes less than 50% of the same device. For ASIC implementations, this configuration will consume approximately 70 kgates, excluding embedded RAM blocks. LEON3 also includes support for multi-processor systems with up to 8 processor cores per AHB bus.

2.2 LEON3-FT-RTAX

The LEON3-FT-RTAX device is an implementation of the LEON3-FT processor using the Actel RTAX-2000S anti-fuse FPGA. The LEON3-FT-RTAX design is based around the LEON3-FT processor and a number of IP cores from the GRLIP IP library. The design is highly modular, and the configuration used for the SEU tests included 3x GRSPW 80 Mbit/s Spacewire links, a combined PROM/SRAM/SDRAM memory controller with EDAC, an AHB/APB bridge, and a standard set of utility cores including timers, UARTs, 16-bit I/O port, interrupt controller and debug interfaces (figure 1).

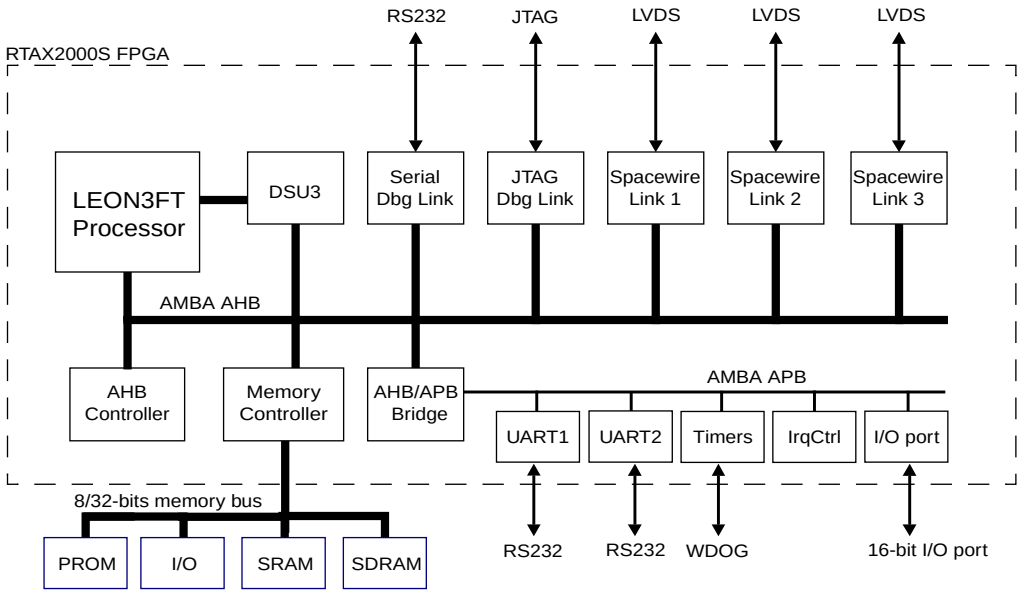

Figure 1. LEON3-FT-RTAX block diagram

2.3 LEON3-FT SEU protection features

The LEON3-FT fault-tolerance features are designed to detect and correct SEU errors in on-chip RAM blocks. The features can be divided in two categories: cache memory protection and register file protection.

The cache memory in LEON3-FT-RTAX consists of separate instructions and data caches, both 8 Kbyte large. Each cache has two parts; tags and data RAM. The tag and data memories are implemented with on-chip block RAMs (RAM64K36) and protected with four parity bits per 32-bit word, allowing to detect up to four simultaneous error per cache word. Upon a detected error, the corresponding cache line is flushed and the instruction is restarted. This operation takes 6 clock cycles and is transparent to software. For diagnostic purposes, error counters are provided to monitor detected and corrected errors in both tag and data parts of the caches.

The processor register file consists of four RAM64K36 blocks and is protected by four parity bits per 32-bit word, plus a duplicated copy of the original data word. Upon a detected parity error, a the duplicate copy of the data is read out from a redundant location in the register file, replacing the failed data. This operation takes place during the normal pipeline operation, and does not require a pipeline restart. The data correction is transparent to the software and does not incur any timing penalty. If the redundant data also contain errors, a register-file error-trap is generated. Error counters are normally provided to monitor register file errors, but were not included in the LEON3-FT-RTAX implementation used during the SEU tests.

3 SEU test setup

3.1 Test system

The target hardware consisted of a GR-CPCI-AX board from Pender Electronic Design, Zurich (figure 3). The board includes one LEON3-FT-RTAX device connected to one SRAM and one SDRAM memory bank. The LEON3-FT-RTAX device operates at 20 MHz using an external oscillator. The board communicates with a host system over one of the LEON3-FT-RTAX on-chip UARTs. The host system consists of a laptop PC running a monitoring software (figure 2).

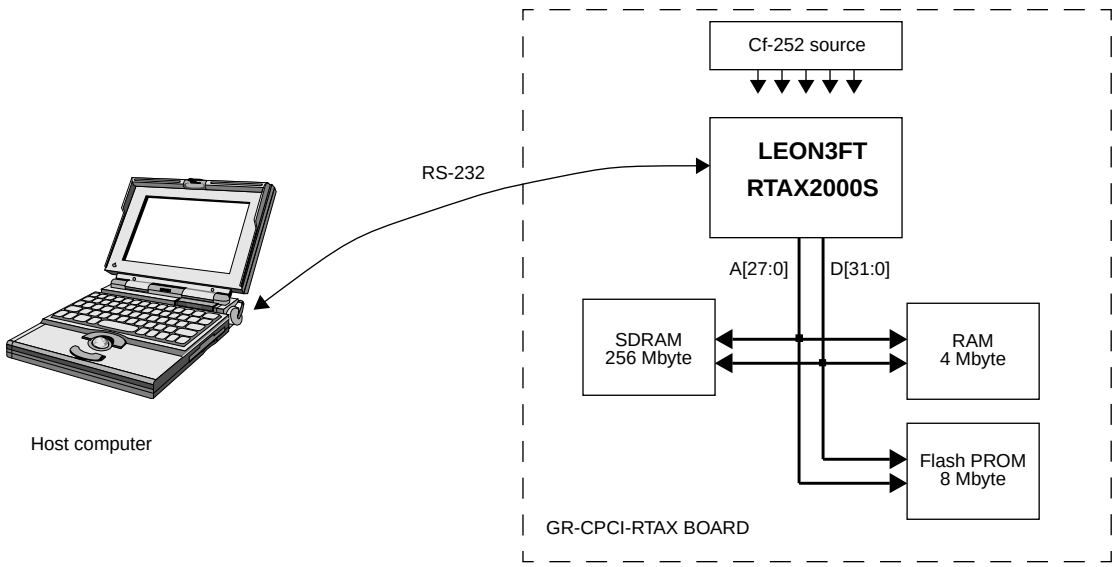

Figure 2. Test system architecture

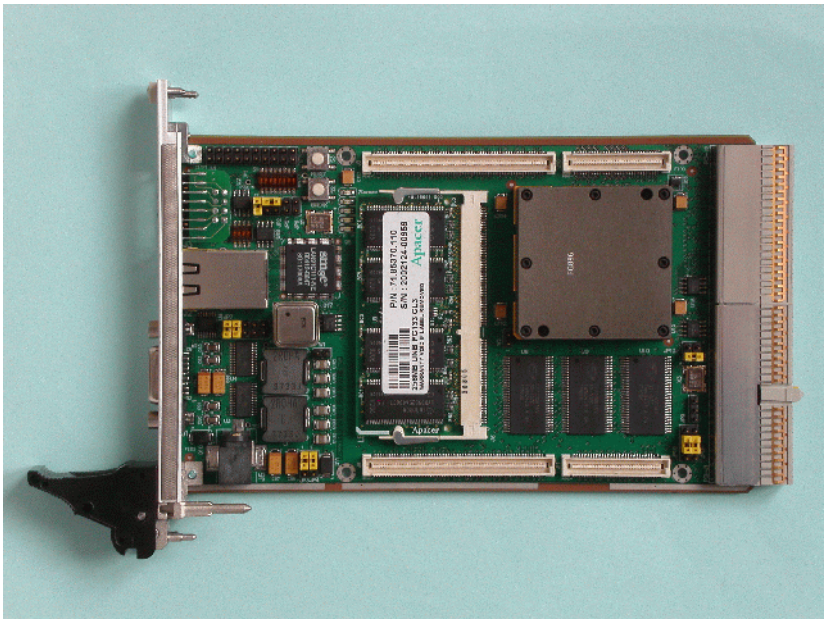

Figure 3. GR-CPCI-RTAX Development board (Pender, 2005)

3.2 Test execution

The LEON3-FT-RTAX device was de-lidded and mounted in a LGA624 socket before the start of the SEU testing (figure 4). The Cf-252 source was placed directly on top of the socket, at a distance of 9 mm from the device. Based on the decay of the source and the distance to the device, the ion flux at the device surface was calculated to ~ 20 particles/s/cm2. The GR-CPCI-RTAX board with the LEON3-FT-RTAX device was inserted into a vacuum chamber, and the Cf-252 source was placed directly on top of the LEON3-FT-RTAX socket. The vacuum chamber was evacuated to the level of 10E-2 mBar, after which the target software was started. The SEU irradiation was maintained for 168 hours (one week), with constant monitoring through the external host system. Each SEU event was registered and stored in a test log together with a time stamp:

```
EC004  1133770473 Mon Dec  5 09:14:33 2005
EC040  1133770515 Mon Dec  5 09:15:15 2005
EC010  1133770639 Mon Dec  5 09:17:19 2005
EC001  1133770900 Mon Dec  5 09:21:40 2005
```

At the end of the test, the host system printed the final error count:

```
!  Successful runs  : 1163865
!  Corrected errors :  2429
!  ite: 123  ide: 200  dte: 258  dde: 1848  rfe: 0
!  Ratio unhandled  :     0%
!  Test ended at Mon Dec  5 11:12:30 2005
```

Figure 4. De-lidded RTAX2000S device in LGA624 socket

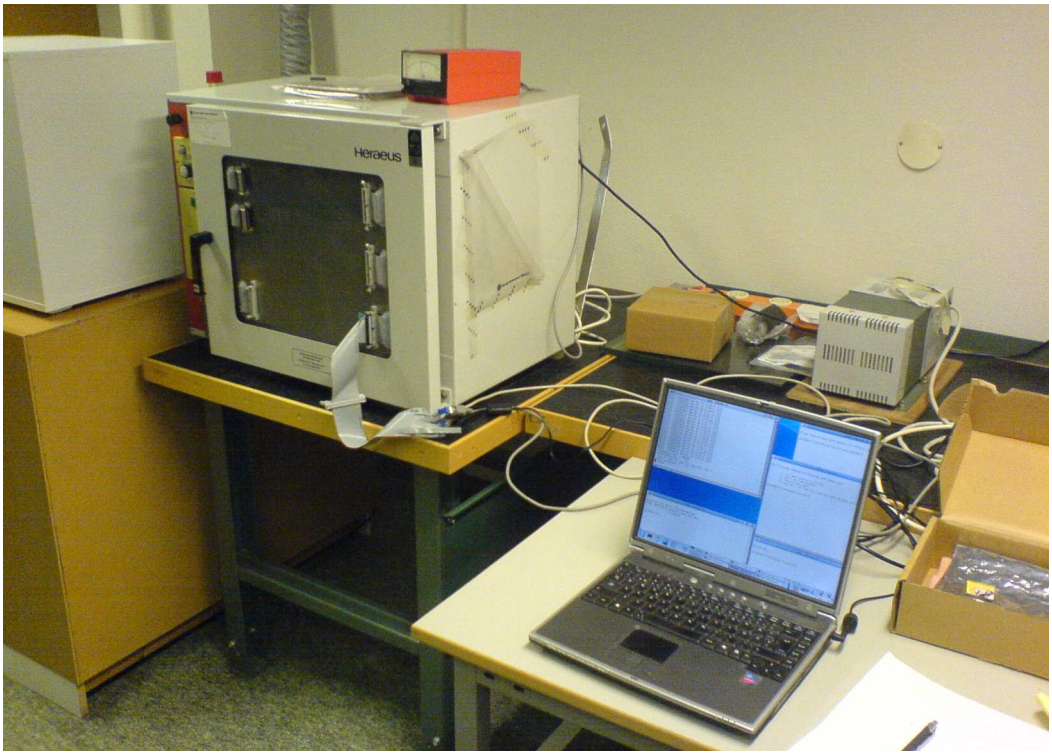

Figure 5. Vacuum chamber and host system

3.3 Target software

During the SEU tests, a special ‘IU-test’ program was executed continuously on the target. The IU-test program is a synthetic application designed to access all on-chip memory (caches and register file). It operates in four steps: a data array with the size of the data cache is allocated and initialized with predefined contents (1), a checksum is calculated by summing the contents of the array (2), the checksum is compared against a pre-calculated value (3), the result (equal or not equal) is sent to the host system over the UART channel. Since the allocated data array has the same size as the data cache, all locations of the data cache will be access during each iteration.

The calculation of the checksum is done with discrete statements rather than a short loop. The code size for the checksum routine is thereby large enough to utilize the full instruction cache during each iteration. To test all registers in the register file, a recursive routine is called periodically. The recursion is 13 levels deep and guarantees that all register windows will be written to memory and then restored again. The IU-test program thus achieves near 100% coverage of all on-chip memory during each iteration of the software.

3.4 Error classification and reporting

The used LEON3-FT-RTAX contained counters that increment each time an error in the cache memories is detected and corrected. These counters are periodically polled by the target run-time system and transmitted to the host system via the UART channel. Anomalies such as unexpected traps or system hangs are also reported to the host system by the target run-time system, either using the UART channel or by a time-out mechanism.

Reported errors and anomalies are classified into two categories, corrected and uncorrected. The corrected errors are formed by summing the reported error counters from the cache memories. All other events such as checksum errors, traps or hangs are considered to be uncorrected errors since they affect the behavior of the application. The host software monitors the reports from the target system and reports a summary after each test run.

4 Results

4.1 Cf-252 SEU test results

The target system was irradiated for exactly 168 hours (one week). During this period, no erroneous calculations, traps or other anomalies were observed. By monitoring the on-chip error counters, a total of 2,429 SEU errors had been detected in the on-chip cache RAM and corrected by the FT logic. The number of corrected errors in the register file could not be measured as it lacked an error counter. Table 1 below shows how the 2,429 errors were divided on the cache memory blocks:

TABLE 1. LEON3-FT-RTAX Cf-252 SEU Error distribution

Module	Errors	RAM bits	Error/bit	Ratio of all errors
Instruction tags	123	8448	0.0146	5.00%
Instruction data	200	73728	0.0027	8.20%
Data tags	258	8448	0.0305	10.60%
Data data	1848	73728	0.0251	76.10%
Total	2429			

From table 1, it can been seen that the majority of effective errors are occurring in the data cache (87%). This can be explained from to the way the IU-test program behaves. The program allocates an array of the size of the data cache, and then calculates a checksum from the array contents. The data cache hit rate is high, and the data cache contents is rarely reloaded due a cache miss. This means that latent (not yet detected) errors are rarely overwritten, and any induced SEU error will be detected and corrected. The code size of the IU-test program on the other hand, is larger than the instruction cache and the cache contents is gradually replaced due to cache misses. This means that latent errors in the instruction cache are frequently overwritten by the normal refill operation and never become effective.

4.2 Simulated SEU error injection

To determine the ratio of effective errors with respect to all injected SEU errors, the target system was also subjected to simulated SEU testing. The target system was running the same software as during the Cf-252 tests, but errors were injected through the LEON3 debug interface, using the GRMON debug monitor. The LEON3 on-chip debug support functions allows diagnostic access to any RAM or register location, and GRMON has built-in functions to insert random errors during program execution. To insert an error, GRMON temporarily halts the processor, injects an error by inverting the target RAM cell, and the releases the processor again. The error injection process takes less than 5 mS, and does not affect the program flow or final error coverage. An error injection test set was created with 3,899 errors randomly distributed over time (800 minutes) and RAM location. All RAM bits were given the same error probability when the set was created. The error set was injected, and the effects were monitored the same way as during the Cf-252 tests.

TABLE 2. LEON3-FT-RTAX Simulated SEU Error distribution

Module	Injected Errors	Effective Errors	Injected/Effective	Ratio eff. errors
Instruction tags	176	176	100 %	7.8 %
Instruction data	1794	375	21 %	17 %
Data tags	181	181	100 %	8.0 %
Data data	1748	1518	87 %	67 %
Total	3899	2250	58 %	

The results from the simulated error injection (table 4) correspond reasonably well with the results obtained with Cf-252 error injection, with the majority of the errors were manifested in the data cache (75%). An interesting observation is that the ratio between injected and effective errors in the data tag memories is 1, i.e. all injected tag errors become effective. This depends on the design of the cache hit logic - when the cache is accessed, the tag is checked for parity errors before being compared to the data address. This means that all tag errors will sooner or later be detected if the application uses the full cache area.

4.3 RAM cross-section

Based on the fact that the error coverage is near 100% for errors in the data tags, it is possible to calculate the approximate SEU cross-section (= sensitive area) for the block RAM cells. The Cf-252 flux at the device surface has been determined to ~ 22 ions/s/cm2, and the following equation can be used:

Xsect = ErrorNum / (ExposureTime * Cf252Flux)

=> 258 / (168 * 60 * 60 * 22) = 1.94 E-5 cm^2 / 8448 bits

=> **2.3E-9 cm^2/bit**

To assess the validity of the obtained cross-section, it can be compared against the values obtained by Actel during the heavy-ion tests of RTAX2000S at the BNL and TAMU Cyclotron facilities (figure 6).

The energy (particle LET) of Cf-252 is 42 MeV/mg/cm2 at the device surface, but decreases with charge collection depth. The average (effective) LET is typically 25 - 35 Mev/mg/cm2, and the measured Cf-252 cross-section correlates well with the BNL/TAMU results which indicates ~ 2E-9cm^2/bit for an LET of 35 MeV/mg/cm^2.

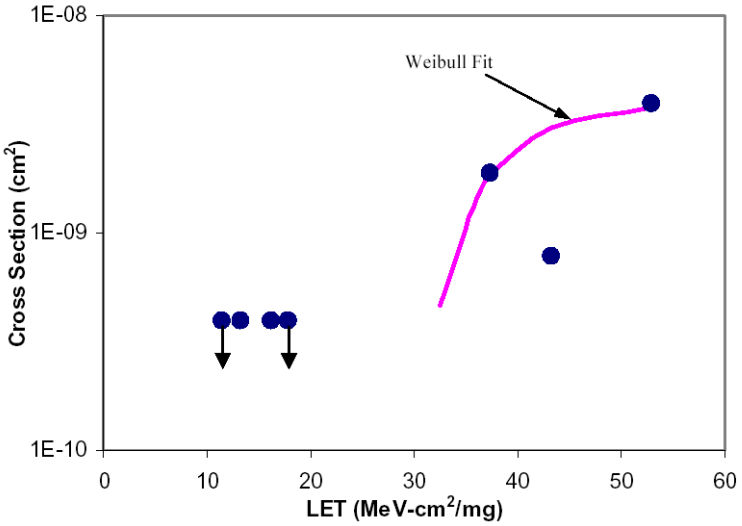

Figure 6. RTAX2000S RAM cell cross-section measurement (J.Wang - Actel, 2004)

5 Conclusions

The LEON3-FT-RTAX processor was submitted to heavy-ion error injection using Cf-252. The error-injection campaign lasted for 168 hours, and the processor executed the application software without any failures, traps or other anomalies. The on-chip error monitoring logic registered a total of 2,429 SEU errors in the cache RAM, all which were properly detected and corrected. The SEU cross-section was determined to 2.3E-9 cm2/bit, well in line with earlier measurements performed by Actel. The overall results shows that the fault-tolerance features included in the LEON3-FT-RTAX processor are well adapted to mitigate the SEU effects encountered in the space environment and provide a fault-free processing platform for both payload and platform applications.