GR1553B

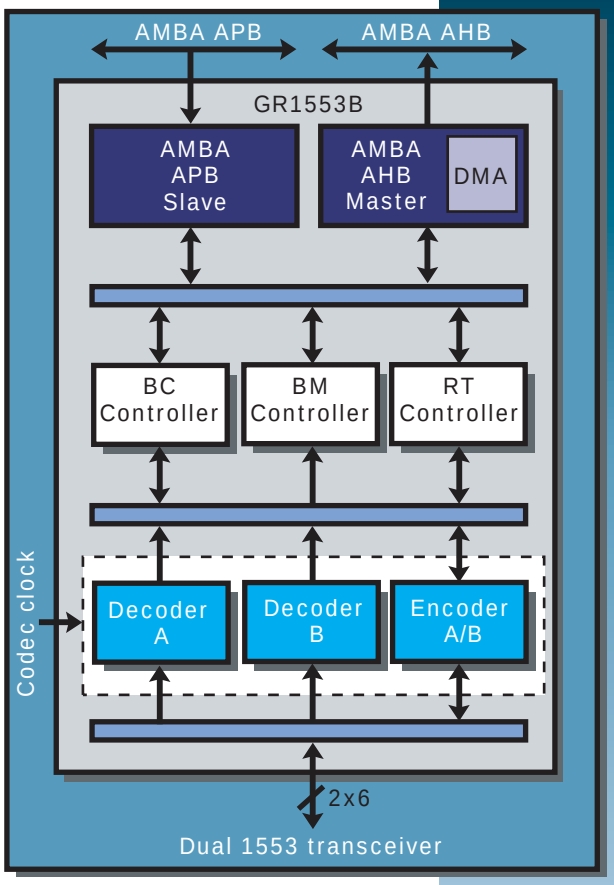
MIL-STD-1553B / AS15531 Interface

AEROFLEX GAISLER

Description

The GR1553B core implements the MIL-STD-1553B (Notice 2) data bus protocol, with ability to serve as Bus Controller (BC), Remote Terminal (RT) or Bus Monitor (BM).

The core is connected to the MIL-STD-1553B bus via a dual transceiver interface (txP/N/en, rxP/N/en). On the system side, the core connects to the AMBA bus as an AHB master for DMA transfers and an APB slave for register access. The core uses a separate 20 MHz clock for the MIL-STD-1553B codec, and runs at any AMBA clock frequency from 10 MHz and upwards.



As Bus Controller, the core works using an automated transfer list concept. The BC supports all permitted transfer types and includes other features such as automatic retries on same or alternating buses, extended RT response timeout for systems with bus repeaters, transfer list looping and branches.

In Remote Terminal mode, the core uses a subaddress table where the user can specify per subaddress whether to accept transmit, receive or broadcast transfers, and maximum transfer size. For storing transfer results and data, linked lists of descriptors are used, with each descriptor pointing to a data buffer.

The Bus Monitor can be run by itself or simultaneously while the core is running as RT or BC. It listens to traffic on the bus and logs the words in a ring buffer. The BM can filter traffic to get only the RT address, subaddress or mode codes of interest, and also log parity and Manchester code errors. All entries in the bus monitor log are time stamped.

Features

- General
  - Implements the MIL-STD-1553B (Notice 2) and SAE AS15531 data bus
  - All transfer types supported, including RT-to-RT and broadcast transfers
  - Dual-redundant bus support
  - Continuous loop-back checking of transmitted MIL-STD-1553B data
  - AMBA (Rev 2.0) AHB master interface, 16-bit aligned data buffers
- Bus Controller
  - Automated transfer list with allocated time slots
  - Synchronized start of transfer list with external pulse
  - Automatic retries on same or alternating buses
  - Secondary transfer list for best-effort, low priority transfers
  - Optional interrupt generation at pre-defined points in transfer list
  - Configurable RT response timeout, up to 44 µs

(Features continue on next page)

Features (continued)

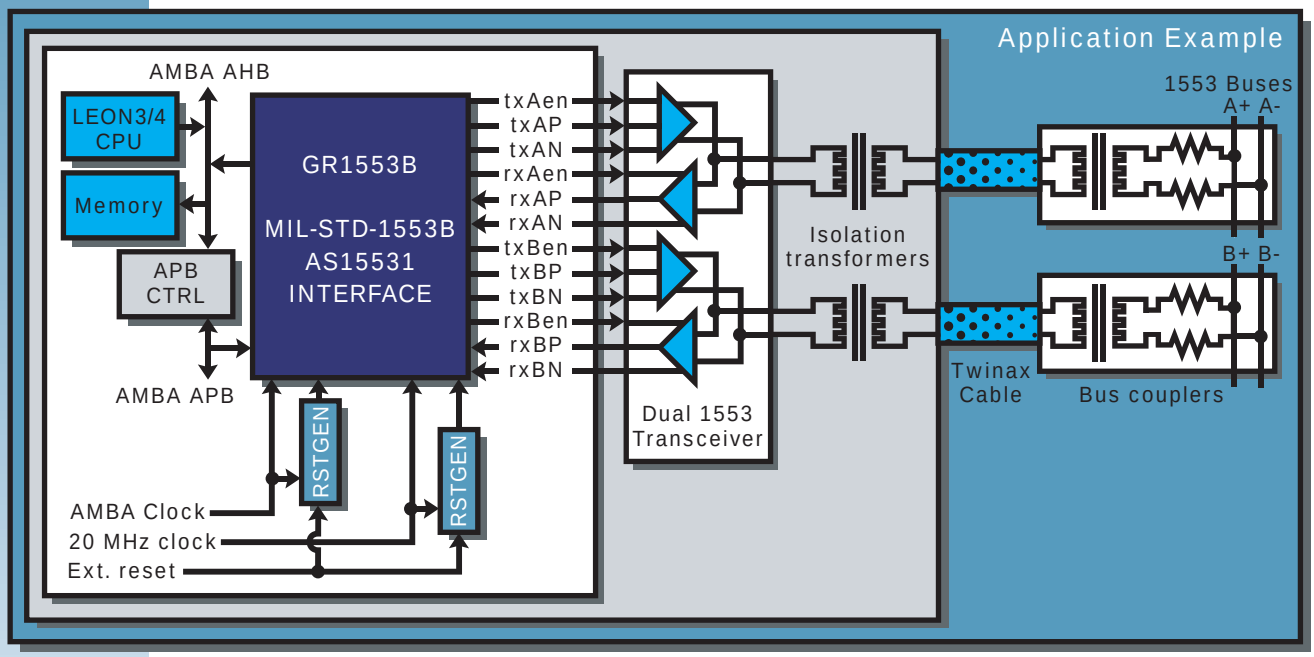
- Remote Terminal
  - Flexible software interface allowing customizable buffering setups
  - Auto wrap-around subaddress capable
  - Time-stamping of transfers
  - Programmable per subaddress maximum transfer size and transmit/receive/broadcast enable
  - Interrupt generation on selected subaddresses
  - Dedicated output that pulses on reception of a synchronize mode code
- Bus Monitor
  - Ring buffer log
  - Filter on address, subaddress, mode codes
  - Can run in parallel with BC or RT

Size and performance

The GR1553B core is inherently portable and can be implemented on most FPGA and ASIC technologies. The core does not use any block RAM:s or FIFO:s.

Approximate resource counts and estimated clock frequencies are shown in the table below.

Device	Actel RTAX	Actel ProASIC3E	Xilinx Virtex2	Xilinx Virtex5	ASIC
Size, RT only	2000C, 1100R	4300 VersaTiles	1800 LUT:s	1500 LUT:s	9000 gates
Size, RT+BC+BM	4700C, 2100R	9800 VersaTiles	4000 LUT:s	3400 LUT:s	20000 gates
AMBA frequency	45MHz	35MHz	80Mhz	100MHz	400MHz



Development boards

Development boards for early development and fast prototyping of systems using the GR1553B core are available, equipped with either Xilinx or Actel FPGA. Each board can be operated either stand-alone or installed as a compact PCI plug-in card.

CONTACT INFORMATION

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