Comparison Between GR716A and GR716B CQFP-132 package

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CHANGE RECORD

Issue	Date	Section / Page	Description
1.0	2022-04-11		First release
1.1	2023-05-24		Clarified precision voltage reference. Updated various fields in comparison table in section 2.2
1.2	2024-08-26		Several updates and clarifications in section 2.1 and 2.2. Added sections 2.4 and 2.5

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1 INTRODUCTION

1.1 Scope of the Document

This document presents the differences between Frontgrade Gaisler's revised GR716B design versus the already existing GR716A device.

The GR716B microcontroller has been developed in an activity with support from the European Space Agency under ARTES Competitiveness & Growth programme. The purpose of the work was to develop a new generation microcontroller, GR716B, based on the GR716A microcontroller.

Important note: This document is provided to highlight the changes/differences between the two microcontrollers, the information in this document is not thorough and complete compared to the information available in the user manuals. The information available in Datasheet and User's manual [RD1] and [RD2] takes precedence over this document.

1.2 Reference Documents

The following documents are referred as they contain relevant information:

[RD1] GR716A Datasheet and User's manual, November 2022, Version 3.2

[RD2] GR716B Advanced Datasheet and User's manual, April 2024, Version 0.7

[RD3] LEON-REX Instruction Set Extension, Frontgrade Gaisler

2 OVERVIEW

2.1 Overview

The GR716B microcontroller has been developed in an activity with support from the European Space Agency under ARTES Competitiveness & Growth programme. The purpose of this activity was to develop an improved microcontroller, GR716B, based on the GR716A microcontroller and to enrich the software ecosystem by industrialization of state-of-the art operating systems, development and simulation tools

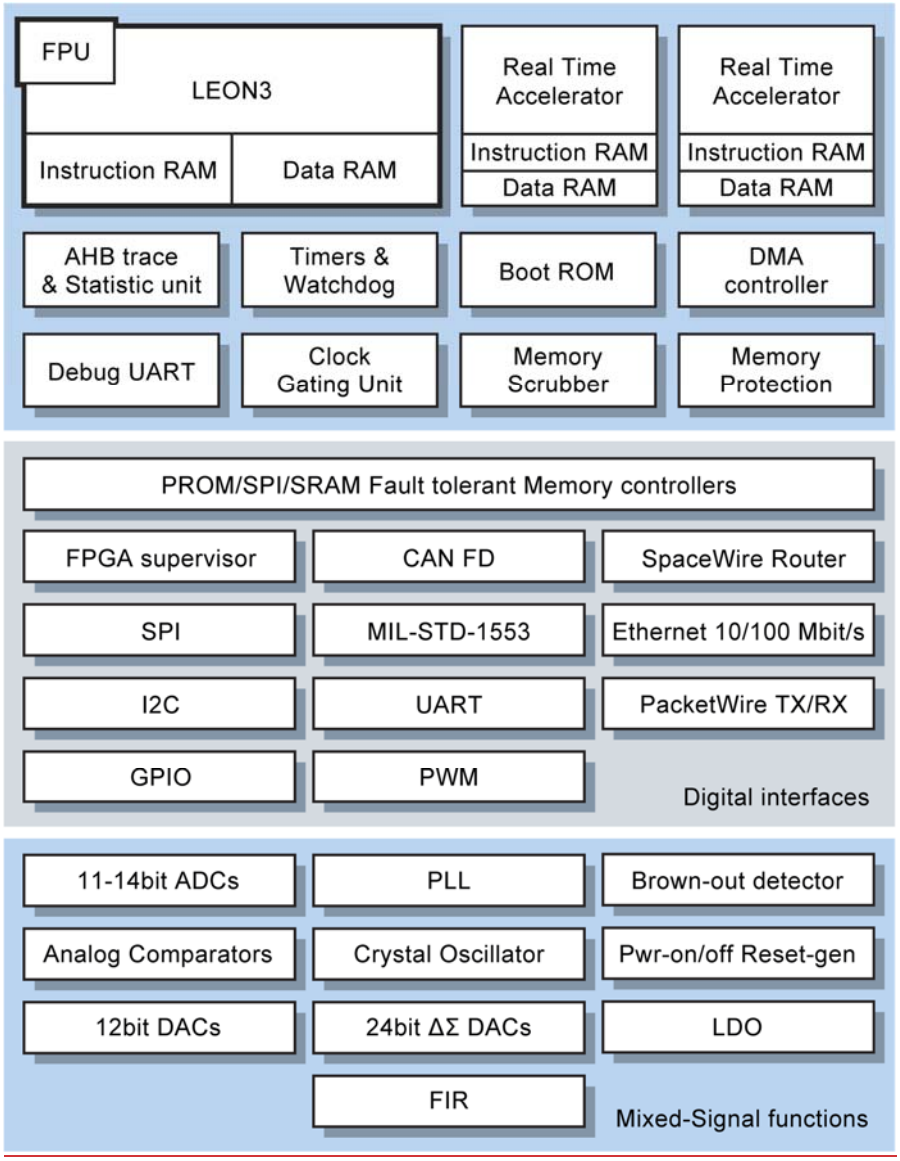


Figure 1 GR716B Block Diagram

The GR716B microcontroller is a single core LEON3FT SPARC V8 processor, with advanced interface protocols, that has been optimized for real-time systems and deterministic software execution. Features such as SPARC V8E Alternate Window Pointer, interrupt zero jitter latency, SPARC V8E multiply step instructions and the possibility to run software (including interrupt handlers) from local RAM are supported to increase the determinism and responsiveness in the system. The LEON-REX instruction set extension is also supported by the microcontroller and is further described in [RD3]. The GR716B also implements two Real Time Accelerators (RTA) whose purpose is to offload the main LEON3FT for simple tasks.

The GR716B architecture is centred around multiple instances of the AMBA Advanced High-speed Bus (AHB), to which the LEON3FT processor and other high-bandwidth units are connected. Low bandwidth peripherals/functions are connected to the AMBA Advanced Peripheral Bus (APB) which is accessed through an AHB to APB bridge. The use of multiple processor buses also enables non-intrusive debugging and the possibility to have direct access to on-board memory without interrupting or involving the LEON3FT processor. 64 external CMOS pins and 5 LVDS transmitters and 4 LVDS

receivers are configurable from software via configuration registers. Pre-defined pin configurations are defined in the boot software and can be enabled by using pull-up/pull-down resistors on external pins during reset. A pre-defined configuration of external pins is useful in cases when the microcontroller should boot from external memories or remote controlled via SpaceWire, CAN FD, UART and SPI after reset. The program controlling the microcontroller needs to set appropriate direction and functionality on all pins after reset depending on the environment that the microcontroller is used in. On-chip LVDS transceivers with support for common-mode, cold-spare and fail-safe for SpaceWire and SPI for Space as well as dedicated pins for external SPI boot ROM boot are available and can optionally be used.

The microcontroller has a high level of integrated analogue functions:

- Analogue to Digital Converters (ADC)
- Brown out detection
- Crystal Oscillator, with external XTAL
- Digital to Analogue Converters (DAC)
- Analogue Comparators
- Power-on and reset functionality
- and Linear Voltage Regulators for single 3.3V supply.

2.2 Comparison

The table below compares GR716A [RD1] and GR716B [RD2]. Differences have been marked in bold text.

Feature	GR716A	GR716B
Availability and Qualification state	Screening tests as per ESCC9000. Lot Qualification as per ESCC2567000/ESCC9000	**Screening and Lot Qualification as per ESCC9000.**
Device ID	0x0716 / 4204	**0x0716 / 4282**
Package	CQFP132	CQFP132
Package Dimension		**D2/E2 dimension is increased by 1.1 mm in the GR716B. See chapter 2.6 for more information**
Power Consumption	< 369mW @ ambient room temperature < 990mW @ 110°C max power use case	**< 570mW@ ambient room temperature** **< TBCmW@ 125°C max power use case**
Supply Voltage	+3V3	+3V3
Temperature range	-55°C to +110°C	-55°C to **+125°C**
Radiation-tolerant	Yes	Yes
User Package Pins	Dedicated SPI memory interface 64 CMOS GPIOs with programmable pull-up / pull-down resistors 3 LVDS transmitters and 3 LVDS receivers	Dedicated SPI memory interface 64 CMOS GPIOs with programmable pull-up / pull-down resistors, **and Schmitt trigger inputs**. **5 LVDS transmitters and 4 LVDS receivers** with **cold-spare, fail-safe** and **extended common mode** support.
Max system frequency	50MHz	**100MHz**
Performance	>70 DMIPS	**Main CPU >140 DMIPS** **RTA 0 >140 DMIPS** **RTA 1 >140 DMIPS**
FPU	Supported	Supported by main CPU
Real Time Accelerator	n/a	**Programmable Real-Time-Accelerators (RTA) improves the overall performance by a factor of 3.**
Internal memory	192KiB	192KiB, **Split between Main CPU and RTA** **Main CPU 128 KiB** **RTA 0 32 KiB** **RTA 1 32 KiB**
External memory interface	SPI, FLASH/SRAM, I2C	SPI, FLASH/SRAM, I2C
Debug Interface	2 port UART	2 port UART
Remote access interface	SpaceWire, UART, SPI, I2C	SpaceWire, **CAN FD (CANOpen)**, UART, SPI, I2C
Boot memory	SPI, FLASH/SRAM, **I2C**	SPI, FLASH/SRAM
SpaceWire	SpaceWire interface	**SpaceWire Router with 2 external ports**

CAN	CAN 2.0	**CAN FD with CANOpen support**
MIL-STD-1553B	Supported	Supported
Ethernet	**n/a**	**10/100Mbit**
FPGA supervisor for programming and scrubbing configuration memory	**n/a**	**Support for Xilinx Virtex5 and Xilinx Kintex Ultra Scale FPGA**
Misc Peripherals	UART, SPI, SPI For Space, I2C	UART, SPI, SPI For Space, I2C
PWM	Programmable PWM interface	**Programmable PWM, including unique configurations for switching-power and motor-control applications.**
DAC	12bit @ 3Msps, 4 channels	12bit @ 3Msps, 4 channels **PWM DAC 24bit, 25MSps, 8 channels**
ADC	Two ADC 11bits @ 200Ksps, 4 differential or 8 single ended	**Four ADC, 11/14bit, 500/80kS/s, 4 differential or 8 single ended.**
External voltage reference	2.4V, maximum load current 2mA	**1.9V, maximum load current 20mA**
Analog comparators	**n/a**	**20 channels, 7 programmable internal comparison levels or external connection.**
FIR Filter	**n/a**	**8 channels, 25MSps, 27 binary programmable taps, configurable from analog comparator etc, e.g. latch-up detection applications.**
DMA	Programmable DMA channels	**Programmable DMA channels with support for 'if-else' statements**
Analog on chip support	Power-on-Reset, Oscillator, Brown-out detection, LVDS transceivers, regulators to support single 3.3V supply	Power-on-Reset, Oscillator, Brown-out detection, LVDS transceivers, regulators to support single 3.3V supply

2.3 Changes in memory map

- General purpose register bank: The address map has been changed between the GR716A and GR716B. The functionality driven by the registers can be different between the devices due to more configurability in the GR716B device
- Analog register configuration: Address map and functionality has changed between the GR716A and GR716B
- New functionality: Configuration registers has been added for new interfaces and functions
- Support for external ADC/DAC interface has been removed

2.4 Changes in pin shared interfaces

- The GR716A and GR716B microcontrollers have 64 external general purpose user input and outputs and LVDS transceivers. All these pins have multiple functionalities. Functionality is selected by the application software during startup and configuration.

The Table 7 IO configuration matrix in [RD1] and [RD2] provides information about the pin shared interfaces. The pin shared interfaces in both the microcontrollers have identical positions in the matrix except for the following deviations

- In GR716B, Analog Applications Pulse Width Modulation (APWM) is included (refer Section 53 in [RD2]) which replaces the previous Pulse Width Modulation Generator (PWM) in GR716A (refer Section 30 in [RD1]). Consequently, the PWM signals are removed from the IO configuration matrix and APWM signals are included in GR716B.
- The redundant SpW interface available through GPIO 21, 22, 23 and 24 (CMOS) in GR716A are removed in GR716B. GR716B has dedicated LVDS transceivers for a redundant SpW interface as well.
- The external ADC, DAC interfaces available in GR716A are removed in GR716B since the functionality is removed in GR716B.
- The test clock outputs available in GR716A GPIO 59 to 63 are moved to GPIO 20 to 23 in GR716B.
- The LVDS pin shared SPI interfaces in GR716B are not pin compatible with GR716A.
- As mentioned in section 2.2 number of additional interfaces are included in GR716B. These interfaces are also part of the I/O switch matrix which makes use of the 64 general purpose user input and outputs and LVDS transceivers.
    - Ethernet, FPGA supervisors (scrubber), additional ADC and Analog Precision Digital Modulator units (APWM_DAC) interfaces are included in GR716B pin shared interfaces.

2.5 Electrical characteristics differences on package pin level

The Electrical characteristics differences between GR716A and GR716B devices at package pin level are listed in the table below.

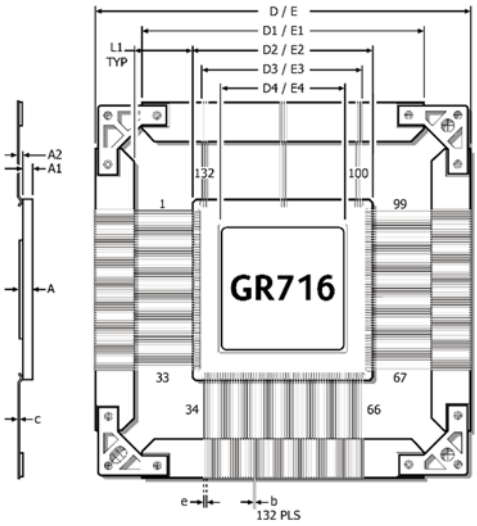
Pkg pin	Signal Name	GR716A	GR716B
2	VDD_LDO	-	Current capability increased
7	DUART_RX	-	30 kohm pulldown
8	DUART_TX	-	Drive capability doubled
12	SPIM_MISO	-	Schmitt trigger
16	RESET_OUT_N	50 kohm pulldown	10 kohm pulldown
17	RESET_IN_N	500 kohm pull to VDD_CORE	100 kohm pull to VDD_CORE
21	GPIO[37]	ADC (x2)	ADC (x3), Analog comparator
22	GPIO[38]	ADC (x2)	ADC (x3), Analog comparator
23	GPIO[39]	ADC (x2)	ADC (x3), Analog comparator
24	GPIO[40]	ADC (x2)	ADC (x3), Analog comparator
25	GPIO[41]	ADC (x2)	ADC (x3), Analog comparator
26	GPIO[42]	ADC (x2)	ADC (x3), Analog comparator
27	GPIO[43]	ADC (x2)	ADC (x3), Analog comparator
28	GPIO[44]	ADC (x2)	ADC (x3), Analog comparator
30	VREFBUF	2.4 V	1.9 V Current capability increased
34	GPIO[45]	DAC	DAC, Analog comparator
35	GPIO[46]	DAC	DAC, Analog comparator
36	GPIO[47]	DAC	DAC, Analog comparator
37	GPIO[48]	DAC	DAC, Analog comparator
40	VDD_LVDS	LVDS I/O supply	LVDS I/O supply and cold-spare activation, for RX[0-3] and TX[0-3]
42	LVDS_TX	LVDS_TX[0]p	LVDS_TX[0]p
43	LVDS_TX	LVDS_TX[0]n	LVDS_TX[0]n
44	LVDS_TX	LVDS_TX[1]p	LVDS_TX[1]p
45	LVDS_TX	LVDS_TX[1]n	LVDS_TX[1]n

46	LVDS_TX or RX	LVDS_TX[2]p	LVDS_TX[2]p or RX[0]p
47	LVDS_TX or RX	LVDS_TX[2]n	LVDS_TX[2]n or RX[0]n
48	LVDS_RX	LVDS_RX[0]p	LVDS_RX[1]p, extended CM
49	LVDS_RX	LVDS_RX[0]n	LVDS_RX[1]n, extended CM
50	LVDS_RX	LVDS_RX[1]p	LVDS_RX[2]p, extended CM
51	LVDS_RX	LVDS_RX[1]n	LVDS_RX[2]n, extended CM
52	LVDS_RX	LVDS_RX[2]p	LVDS_RX[3]p, extended CM
53	LVDS_RX	LVDS_RX[2]n	LVDS_RX[3]n, extended CM
54	SPWCLK	_	Schmitt trigger
57	CLK	_	Schmitt trigger
59	XO_X1 or XO_X2	XO_X1	XO_X2
60	XO_X1 or XO_X2	XO_X2	XO_X1
64	GPIO[49]	_	Schmitt trigger, programmable
65	GPIO[50]	_	Schmitt trigger, programmable
66	GPIO[51]	_	ADC, Analog comparator
67	GPIO[52]	_	ADC, Analog comparator
68	GPIO[53]	_	ADC, Analog comparator
69	GPIO[54]	_	ADC, Analog comparator
70	GPIO[55]	_	ADC, Analog comparator
71	GPIO[56]	_	ADC, Analog comparator
72	GPIO[57]	_	ADC, Analog comparator
73	GPIO[58]	_	ADC, Analog comparator
77	GPIO or LVDS_TX	GPIO[59]	GPIO[59] or LVDS_TX[4]p
78	GPIO or LVDS_TX	GPIO[60]	GPIO[60] or LVDS_TX[4]n
79	GPIO or LVDS_TX	GPIO[61]	GPIO[61] or LVDS_TX[5]p
80	GPIO or LVDS_TX	GPIO[62]	GPIO[62] or LVDS_TX[5]n
81	GPIO[63]	_	Schmitt trigger, programmable
82	GPIO[0]	_	Schmitt trigger, programmable
83	GPIO[1]	_	Schmitt trigger, programmable
84	GPIO[2]	_	Schmitt trigger, programmable
85	GPIO[3]	_	Schmitt trigger, programmable
86	GPIO[4]	_	Schmitt trigger, programmable
90	GPIO[5]	_	Schmitt trigger, programmable

91	GPIO[6]	_	Schmitt trigger, programmable
92	GPIO[7]	_	Schmitt trigger, programmable
93	GPIO[8]	_	Schmitt trigger, programmable
94	GPIO[9]	_	Schmitt trigger, programmable
95	GPIO[10]	_	Schmitt trigger, programmable
96	GPIO[11]	_	Schmitt trigger, programmable
97	GPIO[12]	_	Schmitt trigger, programmable
98	GPIO[13]	_	Schmitt trigger, programmable
99	GPIO[14]	_	Schmitt trigger, programmable
100	GPIO[15]	_	Schmitt trigger, programmable
104	GPIO[16]	_	Schmitt trigger, programmable
105	GPIO[17]	_	Schmitt trigger, programmable
106	GPIO[18]	_	Schmitt trigger, programmable
107	GPIO[19]	_	Schmitt trigger, programmable
108	GPIO[20]	_	Schmitt trigger, programmable
109	GPIO[21]	_	Schmitt trigger, programmable
110	GPIO[22]	_	Schmitt trigger, programmable
111	GPIO[23]	_	Schmitt trigger, programmable
112	GPIO[24]	_	Schmitt trigger, programmable
113	GPIO[25]	_	Schmitt trigger, programmable
114	GPIO[26]	_	Schmitt trigger, programmable
118	GPIO[27]	_	Schmitt trigger, programmable
119	GPIO[28]	_	Schmitt trigger, programmable
120	GPIO[29]	_	Schmitt trigger, programmable
121	GPIO[30]	_	Schmitt trigger, programmable
122	GPIO[31]	_	Schmitt trigger, programmable
123	GPIO[32]	_	Schmitt trigger, programmable
124	GPIO[33]	_	Schmitt trigger, programmable
125	GPIO[34]	_	Schmitt trigger, programmable
126	GPIO[35]	_	Schmitt trigger, programmable
127	GPIO[36]	_	Schmitt trigger, programmable
131	VDD_LDO	_	Current capability increased

2.6 Changes of package body size

Three of the package parameters have been changed to allow new functionalities in the GR716B. Changed parameters are marked with bold text in the table below.



Name	Parameter	GR716A			GR716B			
		Min	Typ	Max	Min	Typ	Max	Unit
A			3.05	3.5		3.05	3.5	mm
A1				2.26	1.84		2.26	mm
A2				0.53	0.27		0.53	mm
b1	Width of lead when closest to case	0.23		0.329	0.23		0.329	mm
b2	Width of lead when closest to ceramic bar	0.15		0.25	0.15		0.25	mm
c		0.075		0.175	0.075		0.175	mm
D/E			50.85			50.85		mm
D1/E1			30.73			30.73		mm
D2/E2 [1)]		23.88		24.26	**25.10**		**25.48**	**mm**
D3/E3			20.32			20.32		mm
D4/E4			20.2			**22.0**		mm
e			0.635			0.635		mm
L1 [1)]	Length of lead from case to ceramic bar (L2+L3)		8.3			**7.75**		mm
L2 [1)]	Length of lead with width b1		7.0			**6.45**		mm
L3	Length of lead with width b2		1.3			1.3		mm
Mass	Mass of case, including the lead frames.		8.5±1			9±0.5		grams

Note 1	Dimension D2/E2 for GR716B is increased by 1.1 mm. To prepare PCB footprint for replacement, it is suggested to adjust the solder pad length accordingly. Dimension L1 and L2 will at the same time be reduced with by up to 0.55 mm.