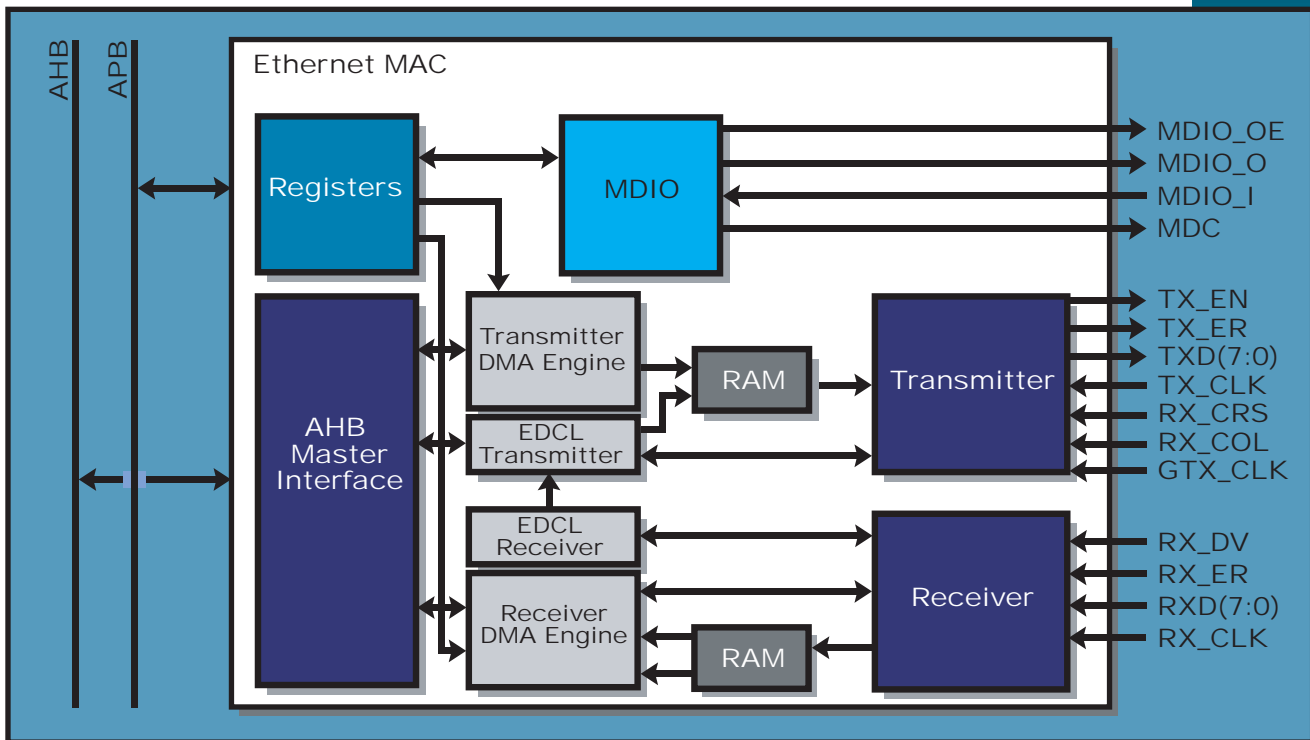


GRETH_GB1T

10/100/1000 Ethernet MAC

Description

The GRETH_GB1T core implements a 10/100/1000 Mbit/s Ethernet Media Access Controller (MAC) with AMBA host interface. The core implements the 802.3-2002 Ethernet standard. Receive and transmit data is autonomously transferred between the Ethernet MAC and the AMBA AHB bus using DMA transfers. Through the use of receive and transmit descriptors, multiple ethernet packets can be received and transmitted without CPU involvement. The GRETH_GB1T provides support for the MII and GMII PHY interfaces. Hardware support is also provided for the EDCL UDP debugging protocol. For critical space applications, a fault-tolerant version of GRETH_GB1T is available with full SEU protection of all RAM blocks.



Features

- AMBA AHB back end with DMA
- Support for Scatter/Gather DMA
- Checksum offloading in hardware for TCP/IP/UDP for both receiver and transmitter
- Descriptor based autonomous multi-packet transfer
- Portable
- Multicast address filtering

Deliverables

- VHDL source code or FPGA/ASIC netlist
- Stand-alone testbench
- Optional plug and play interface for GRLIB IP-library
- User's manual
- Driver for RTEMS, eCos, Linux 2.0, Linux 2.6, VxWorks, ThreadX, LynxOS, Nucleus, and BCC

Size and Performance

The GRETH_GBIT is inherently portable and can be implemented on most FPGA and ASIC technologies. The table shows the approximate area and frequency for two different GRETH_GBIT configurations on Altera Stratix, Xilinx Virtex and ASIC technologies.

(LUTs / Registers / AHB MHz / RAM) Virtex5
(ALMs / M512 / M4K / AHB MHz) Altera

Core configuration	Stratix II	Virtex5	ASIC gates
GRETH_GBIT	2,300 / 1 / 9 / 130	3,800 / 2,100 / 140 / 2	26,000
GRETH_GBIT + EDCL	2,800 / 1 / 11 / 130	4,500 / 2,300 / 140 / 4	32,000

The GRETH_GBIT core can be licensed commercially, either stand-alone or as part of the GRLIB IP library. It is delivered either as VHDL source-code or as a netlist. Evaluation netlists can also be delivered for most technologies.

EDCL

The EDCL is an optional hardware unit providing read/write access to the AHB bus through ethernet using an UDP based protocol. It operates in parallel with the MAC DMA and does not interfere with the normal network traffic other than lowering performance. Speeds up to 500 Mbit/s effective throughput have been achieved when accessing the AHB bus through the EDCL using the GRMON debug monitor.

CONTACT INFORMATION

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