Product Brief

RELEASED NOV 1, 2021

32-BIT SPARC V8 PROCESSOR

# LEON5

The LEON5 is a high-performance dual issue processor conforming to the 32-bit SPARC V8 RISC (Reduced Instruction Set Computer) architecture. The processor is designed as a synthesizable model in VHDL for integration in system-on-chip (SoC) designs on ASIC and FPGA technologies. The LEON5 can be implemented with fault-tolerance features to protect on chip memories and transparently recover from soft errors. The on-chip bus interfaces are compatible with existing IP cores from the GRLIB IP library as well as any custom cores developed for LEON3/LEON4, allowing LEON5 to be used as a drop-in replacement in existing designs.

The internal design of the LEON5 is significantly enhanced compared to earlier LEON generations and achieves over twice the performance of LEON4 (as measured by CoreMark) at the same clock frequency. The main new feature of the LEON5 pipeline is the dual-issue capability, allowing up to two instructions per cycle to be executed in parallel in the processor. To support the increased issue rate of the pipeline, the LEON5 has advanced branch prediction capabilities. The cache controller of the LEON5 supports a store buffer FIFO with one cycle per store sustained throughput, wide AHB bus support to enable fast stores and fast cache refill, as well as several other enhancements. The LEON5 integrates with the GRFPU5 high-performance floating-point unit (FPU). Tightly coupled memory support is available as a synthesis option to provide areas for code and data storage with zero wait-state access (as fast as a cache hit).

The fault-tolerant version of the LEON5 (LEON5FT) implements an innovative patent pending ECC solution that protects against single-bit errors in the on-chip memories as well as detects wider errors that may occur in harsh environments on certain technologies. The LEON5 repairs soft errors in the internal cache memories using an internal correction cycle without any memory access, using re-fetch from memory as a fallback solution for uncorrectable errors. An internal scrubber function is included to prevent error build-up. All correction and scrubbing is transparent to software.

The standard configurations of the LEON5 are listed in the table below. Note that the design is modular and other configurations are possible. Fault tolerance support and Tightly coupled memory can be enabled on top of any of these configurations.

| CONFIGURATION NAME | LEON5-ADV (tentative) | LEON5-HP | LEON-GP | LEON5-MIN |
|---|---|---|---|---|
| **Issue rate** | Dual | Dual | Dual | Single |
| **I-cache** | 4x4KiB | 4x4KiB | 4x4KiB | 1x4KiB |
| **D-Cache** | 4x4KiB | 4x4KiB | 4x4KiB | 1x4KiB |
| **TLB I+D** | 24+24 | 24+24 | 16+16 | 4+4 |
| **FPU** | GRFPU5 | GRFPU5 | GRFPU5 | NanoFPU |
| **Bus** | Multi-AHB *** | AHB | AHB | AHB |
| **Bus data width** | 32 - 128* | 32 - 128* | 32 - 128* | 32 - 128* |
| **HW virt** | Yes *** | No | No | No |
| **L2 cache and IOMMU** | Yes *** | No** | No** | No** |

* Wide interface compatible also with 32-bit AHB masters and slaves
** L2 cache/IOMMU can be added externally as separate cores
*** Feature currently under development

SPARC Compliant SCD V8

GRLIB SYSTEM-ON-CHIP IP LIBRARY

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**Features:**

- SPARC V8 instruction set with V8e extensions and compare-and-swap
- Advanced dual-issue pipeline with Late ALU, Dynamic Branch Prediction and Branch Target Buffer to maximize instruction per cycle (IPC) throughput
- Hardware floating-point support and Hardware multiply and divide units
  - Non-pipelined area efficient FPU (NanoFPU) or High-performance, fully pipelined IEEE-754 FPU including hardware support for denormalized numbers (GRFPU5)
- Separate instruction and data L1 cache (Harvard architecture) with snooping
- SPARC Reference MMU (SRMMU) with TLB
- AMBA-2.0 AHB bus interface, 32-, 64- or 128-bit wide
  - Subsystem including processor and Level-2 cache with AXI4 backend also available
- Advanced on-chip debug support with instruction and data trace buffer, and performance counters
- Symmetric Multi-processor support (SMP) with cache coherency
- Power-down mode and clock gating
- Robust and fully synchronous single-edge clock design
- High performance:
  - Dhrystone*: 3.23 DMIPS/MHz (-O3, inlining allowed)
  - Coremark* : 4.52 CoreMark/MHz (-O3,-funroll-all-loops -finline-functions -finline-limit=1000)

* All the results generated using BCC 2.0.7 toolchain

**Synthesis:**

The LEON5 processor can be synthesized with common synthesis tools such as Xilinx Vivado, Synplify, and Synopsys DC. The processor model is highly portable between different implementation technologies.

**Software development:**

Being SPARC V8 conformant, compilers and kernels for SPARC V8 can be used with LEON5 (kernels will need a LEON BSP). To simplify software development, we provide several toolchains and operating systems.

Debugging is generally done using the GDB debugger, and a graphical front-end such as DDD or Eclipse. The GRMON monitor interfaces to the LEON5 on-chip debug support unit (DSU), implementing a large range of debug functions. The LEON5 processor will also be supported by our TSIM3 simulator.

**Software compatibility:**

LEON5 provides backward compatibility for software designed for LEON3 and LEON4 systems and can in most cases run existing binaries unmodified. LEON5 runs bare-C (BCC2), RTEMS, VxWorks and Linux.

**Availability:**

The LEON5 is immediately available and a version without the pipelined GRFPU5 and without fault-tolerance features is part of the free open source GRLIB IP library gaisler.com/getgrlib

Pre-built evaluation bitstreams are available for FPGA development boards.
Please see gaisler.com/LEON5 for more information.