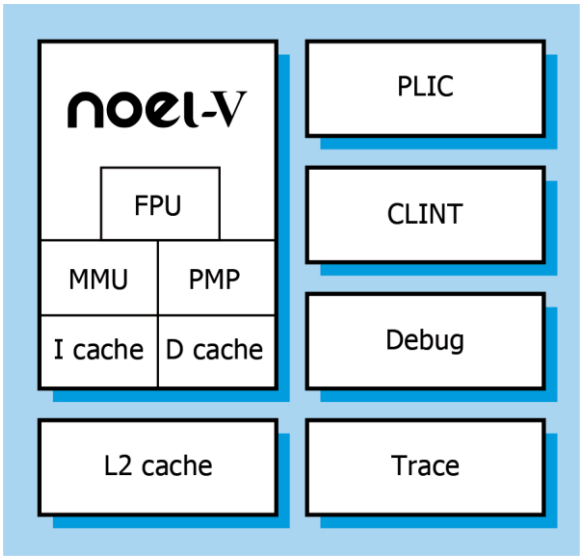
Product Brief

AUGUST 2022

NOEL-V: Highly configurable RISC-V processor

- Suitable for both FPGA and ASIC
- Optional fault tolerant features for space applications
- Multi core support (SMP/AMP)
- 32-bit or 64-bit architecture
- Dual-issue, 7-stage pipeline
- Hypervisor extension for virtualization
- Native AMBA 2.0 AHB bus interface
- Subsystem including L2 cache with AHB or AXI backend also available
- Area efficient or high performance FPU



The NOEL-V has several example configurations listed in the table below. It is also possible to tailor additional configuration settings to create custom processor configurations. All configurations are available in 32 and 64 bits architecture.

Configuration	Target	Pipeline	RISC-V extensions	MMU	PMP	Privilege modes	Example SW
HP	High performance	Dual Issue	IMAFDCHB*	Yes	Yes	Supervisor, User and Machine + Virtualization	Hypervisor, Linux, VxWorks
GP	General Purpose	Dual or single issue	IMAFDCHB*	Yes	Yes	Supervisor, User and Machine	Linux, VxWorks
GP-lite	General purpose Area optimized	Dual or single issue	IMAFDCB*	Yes	No	Supervisor, User and Machine	Linux, VxWorks
MC	Controller applications	Single issue	IMAFDCB*	No	Yes	User and Machine	RTEMS
MC-lite	Controller applications Area Optimized	Single issue	IMA	No	No	User and Machine	RTEMS

*Only parts of the B extensions may be enabled for this configuration.

RISC-V Extensions:
I - Base Integer instructions
M - Hardware support for Multiply and Division
A - Atomics
FD - Single/Double Floating Point
C – Compressed (16 bits) instructions
H - Hardware hypervisor support
B – Bit Manipulation support

Product Brief

AUGUST 2022

RISC-V PROCESSOR IP CORE

NOEL-V

The NOEL-V processor model implements open standards developed within RISC-V International and allows SoC designers to leverage the peripherals and example designs that are provided with the GRLIB IP library. The processor core is also available in a fault-tolerant version where on-chip memories are protected against radiation effects and where radiation induced errors are handled without software interruptions.

The NOEL-V can run complex operative systems providing performance comparable to an ARM Cortex A53. In its most performant configuration, the NOEL-V is implemented as a dual-issue processor, allowing up to two instructions per cycle to be executed in parallel. In such configuration, the NOEL-V achieves 4.03** / 4.69*** CoreMark/MHz.

To support the instruction issue rate of the pipeline, the NOEL-V has advanced branch prediction capabilities. The write-through Level-1 cache has a wide bus interface, supporting fast cacheline fills, and a store-buffer.

Synthesis:	The NOEL-V processor can be synthesized with common synthesis tools such as Xilinx Vivado, Synplify, and Synopsys DC. The processor model is highly portable between different implementation technologies. The processor is delivered with example designs for many common boards and FPGA technologies.
Software development:	The NOEL-V processor implements the RISC-V ISA which means that compilers and kernels for RISC-V can be used with NOEL-V (kernels will need a NOEL-V BSP). To simplify software development, we provide several prebuilt toolchains.
Availability:	The NOEL-V is immediately available. A version without the pipelined FPU and without fault-tolerance features is part of the free open source GRLIB IP library gaisler.com/getgrlib Pre-bult evaluation bitstreams are available for FPGA development boards. Please see gaisler.com/NOEL-V for additional information.

**-march=rv64im -mabi=lp64 -O2 -funroll-all-loops -funswitch-loops -fgcse-after-reload -fpredictive-commoning -mtune=sifive-7-series -finline-functions -fipa- cp-clone -falign-functions=8 -falign-loops=8 -falign-jumps=8 --param max-inline-insns-auto=20 using GCC 9.2.0 under RTEMS 5

*** Using "#define ee_u32 int32_t" in core_portme.h, as is common for 64 bit RISC-V.