Product Brief

RELEASED NOV 1, 2021

RISC-V PROCESSOR IP CORE

NOEL-V

The NOEL-V is a synthesizable VHDL model of a processor that implements the RISC-V instruction set architecture. The IP core is suitable for both FPGA and ASIC implementations and is part of a subsystem where users select from a set of standard configurations to meet application needs and adapt to target technology constraints. NOEL-V can be implemented as a 32-bit (RV32) or 64-bit (RV64) processor.

The NOEL-V processor model implements open standards developed within RISC-V International and allows SoC designers to leverage the peripherals and example designs that are provided with the GRLIB IP library. The processor core is also available in a fault-tolerant version where on-chip memories are protected against radiation effects. This allows designers to create radiation hardened microprocessor implementations.

In its most performant configuration, the NOEL-V is implemented as a dual-issue processor, allowing up to two instructions per cycle to be executed in parallel. To support the instruction issue rate of the pipeline, the NOEL-V has advanced branch prediction capabilities. The write-through Level-1 cache has a wide bus interface, supporting fast cacheline fills, and a store-buffer.

The NOEL-V processor core is available as part of a subsystem that also contains system peripherals. The subsystem can be configured to use the processor configurations listed in the table below. It is also possible to tailor additional configuration settings to create custom processor configurations by editing the VHDL generic (configuration parameter) assignments in the subsystem.

CONFIGURATION	ISA*	Pipeline	Cache	MMU	PMP	FPU	NOTE
TIN32	RV32IM	single issue	no	no	no	no	Tiny configuration
MIN32	RV32IMAC	single issue	yes	no	yes	no	Minimal 32-bit configuration
MIN64	RV64IMAC	single issue	yes	no	yes	no	Minimal 64-bit configuration
GPP32	RV32GCH	single or dual issue	yes	yes	yes	GRFPUnv or NanoFPUnv	General purpose 32-bit configuration
GPP64	RV64GCH	single or dual issue	yes	yes	yes	GRFPUnv or NanoFPUnv	General purpose 64-bit configuration
HPP32	RV32GCH	dual issue	yes	yes	yes	GRFPUnv or NanoFPUnv	High-performance 32-bit configuration
HPP64	RV64GCH	dual issue	yes	yes	yes	GRFPUnv or NanoFPUnv	High-performance 64-bit configuration

Note: Configurations were updated 2021-Mar-04
Note*: Key for ISA column:

- RV32I - 32-bit Base Integer instructions
- RV64I - 64-bit Base Integer instructions
- M - Hardware support for multiply and division
- A - Atomics
- FD - Single/Double Precision Floating Point
- G - short for IMAFD
- C – Compressed instructions
- H - Hardware hypervisor

Note: The standard configurations may be extended when additional extensions are supported by NOEL-V. For example, the Zbb extension may become part of the standard configurations in the future.

GRLIB SYSTEM-ON-CHIP IP LIBRARY

RISC-V®

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Features:

- RISC-V 32-bit and 64-bit architecture
- Hardware multiply and divide units
- Compressed (16 bit) instructions
- Atomic instruction extension
- Hypervisor extension
- 32/64 bit floating point extensions using non-pipelined area efficient FPU or high-performance pipelined FPU
- Machine, supervisor and user mode. RISC-V standard MMU with configurable TLB.
- RISC-V standard PLIC
- RISC-V standard PMP (physical memory protection)
- RISC-V standard external debug support
- Advanced dual-issue in-order pipeline
- Dynamic branch prediction, branch target buffer and return address stack
- Four full ALUs, two of them late in the pipeline to reduce stalls
- Separate instruction and data L1 cache (Harvard architecture) with snooping
- Optional L2 cache: 256-bit internal, 1-4 ways, 16 KiB - 2 MiB
- Native AMBA 2.0 AHB bus interface, 32-, 64- or 128-bit wide.
- Subsystem including processor and Level-2 cache with AXI4 backend also available.
- Robust and fully synchronous single-edge clock design
- Extensively configurable
- Large range of software tools: compilers, kernels and debug monitors
- High Performance*: CoreMark: 4.03** / 4.69*** CoreMark/MHz

*For HPP64 configuration. CoreMark score varies with processor configuration, microarchitectural changes, and toolchains. The CoreMark score is preliminary and will be updated for future milestones.
**-march=rv64im -mabi=lp64 -O2 -funroll-all-loops -funswitch-loops -fgcse-after-reload -fpredictive-commoning -mtune=sifive-7-series
-finline-functions -fipa-cp-clone -falign-functions=8 -falign-loops=8 -falign-jumps=8 --param max-inline-insns-auto=20 using GCC 9.2.0 under RTEMS 5
*** Using "#define ee_u32 int32_t" in core_portme.h, as is common for 64 bit RISC-V.

Synthesis:

The NOEL-V processor can be synthesized with common synthesis tools such as Xilinx Vivado, Synplify, and Synopsys DC. The processor model is highly portable between different implementation technologies.

Software development:

The NOEL-V processor implements the RISC-V ISA which means that compilers and kernels for RISC-V can be used with NOEL-V (kernels will need a NOEL-V BSP).
To simplify software development, we provide several prebuilt toolchains.

Availability:

The NOEL-V is immediately available. A version without the pipelined FPU and without fault-tolerance features is part of the free open source GRLIB IP library
gaisler.com/getgrlib

Pre-bult evaluation bitstreams are available for FPGA development boards.
Please see gaisler.com/NOEL-V for additional information.